# TFE 4200 Analog Integrated Circuits

Problem sheet #4

#1. The op-amp configured in the non-inverting mode shown in the Fig. 1 has the following parameters.

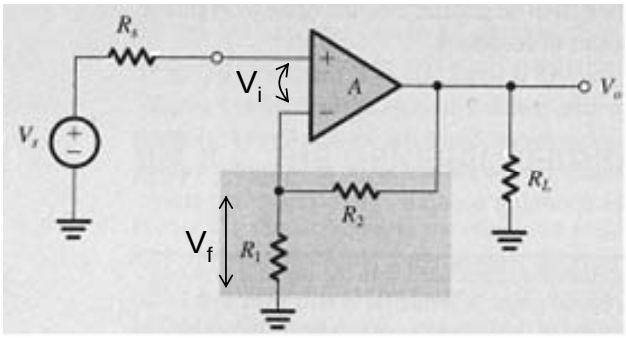


Fig. 1

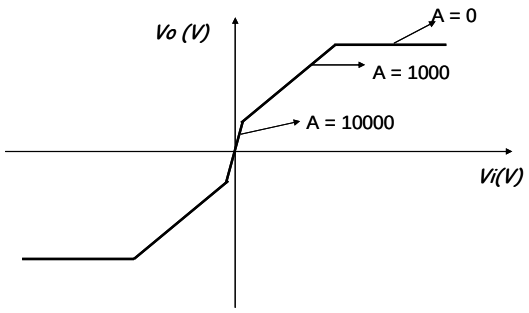


Fig. 2

Open loop voltage gain(A) = $10^3$
-20dB per decade roll off at high frequencies with $f_{-3dB}$ = 100Hz
Input impedance of the op-amp: Infinite
Output impedance of the op-amp: Zero

a). Find the expression for feedback factor ($\beta$) and find the ratio of R2/R1 to obtain a closed loop gain ($A_f$) of 10. [HINT: R2/R1 should be close to 9]
b). What is the amount of feedback ($1+A\beta$) in decibels? If $V_S$ = 1V, find Vo, $V_f$ and $V_i$. If open-loop voltage gain (A) decreases by 25%, what is the corresponding decrease in the closed loop voltage gain ($A_f$)? Write your comments. [HINT: decrease in closed loop gain should be around 0.25%]
c). What is the 3-dB frequency of the closed loop amplifier? Compare it with the 3-dB frequency of the amplifier without feedback.
[HINT: 3-dB frequency of closed loop amplifier should be around 10KHz]
#2. Fig. 2 shows an amplifier transfer characteristic without feedback. Draw the transfer characteristic for the closed loop amplifier with $\beta$ = 0.01. Compare it with the transfer characteristic of the amplifier without feedback. Comment on the nonlinear distortion.
[HINT: Find the closed loop gain to draw the transfer characteristic for closed loop case]
#3. A series-shunt feedback circuit employs a basic voltage amplifier that has a dc gain of $10^4$ V/V and an STC frequency response with a unity-gain frequency of 1 MHz. The input resistance of the basic amplifier is 10K$\Omega$ and it's output resistance is 1K$\Omega$. If the feedback factor $\beta$=0.1 V/V, find the input impedance $Z_{if}$ and the output impedance $Z_{of}$ of the feedback amplifier. Also find the values of each impedance at $10^3$ Hz and at $10^5$ Hz.[ANS: $Z_{of}$=10$\Omega$@1KHz,706$\Omega$@100KHz]

#4. A series-series feedback amplifier (shown in Fig. 3) employs a transconductance amplifier having $G_m$ = 100mA/V, input resistance of 10kΩ, and output resistance of 100kΩ. The feedback network has β = 0.1 V/mA, an input resistance (with port 1 open circuited) of 100Ω, and output resistance (with port 2 open circuited) of 10kΩ. The amplifier operates with a signal source having a resistance of 10kΩ and with a load resistance of 10kΩ. Find $A_f$, $R_{in}$, and $R_{out}$.
[ANS: $A_f$ = 7.53 mA/V, $R_{in}$ = 110.81 KΩ, $R_{out}$ = 433.37 KΩ]

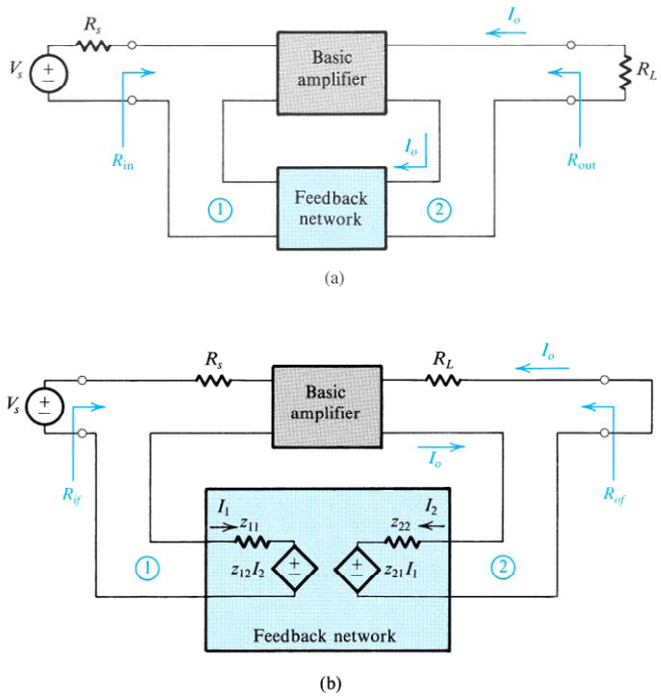


Fig. 3

#5. Find the voltage gain Vo/Vs, the input resistance $R_{in}$, and the output resistance $R_{out}$ of the inverting op-amp configuration shown in Fig. 4. The op-amp has open-loop gain of $10^4$ V/V, $R_{id}$ = 100 kΩ, and ro = 1 kΩ.

[HINT: feedback is shunt-shunt type]

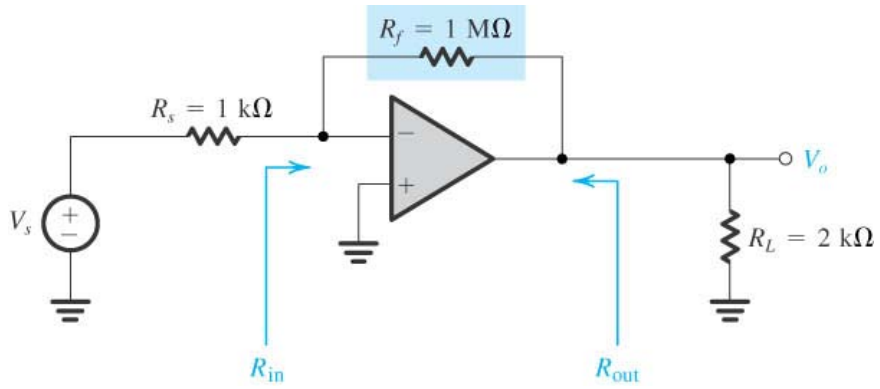


Fig. 4

#6. Negative feedback is to be used to modify the characteristics of a particular amplifier for various purposes. Identify the feedback topology to be used if:

a). Input resistance is to be lowered and output resistance to be raised
b). Both input and output resistance to be raised
c). Both output and input resistances are to be lowered
d). Input resistance is to be raised and output resistance to lowered

#7 a). Plot the voltage gain of the circuit (input: VSIG, output: VOUT) in Figure 5.1 as a function of the frequency. Determine the -3 dB bandwidth of the circuit. The netlist of the circuit is given at the end (This is the same circuit as in Exercise 3, problem 7). The low-frequency voltage gain should be approximately Au=Vout/Vin=28 with VDCIN=1.2V.

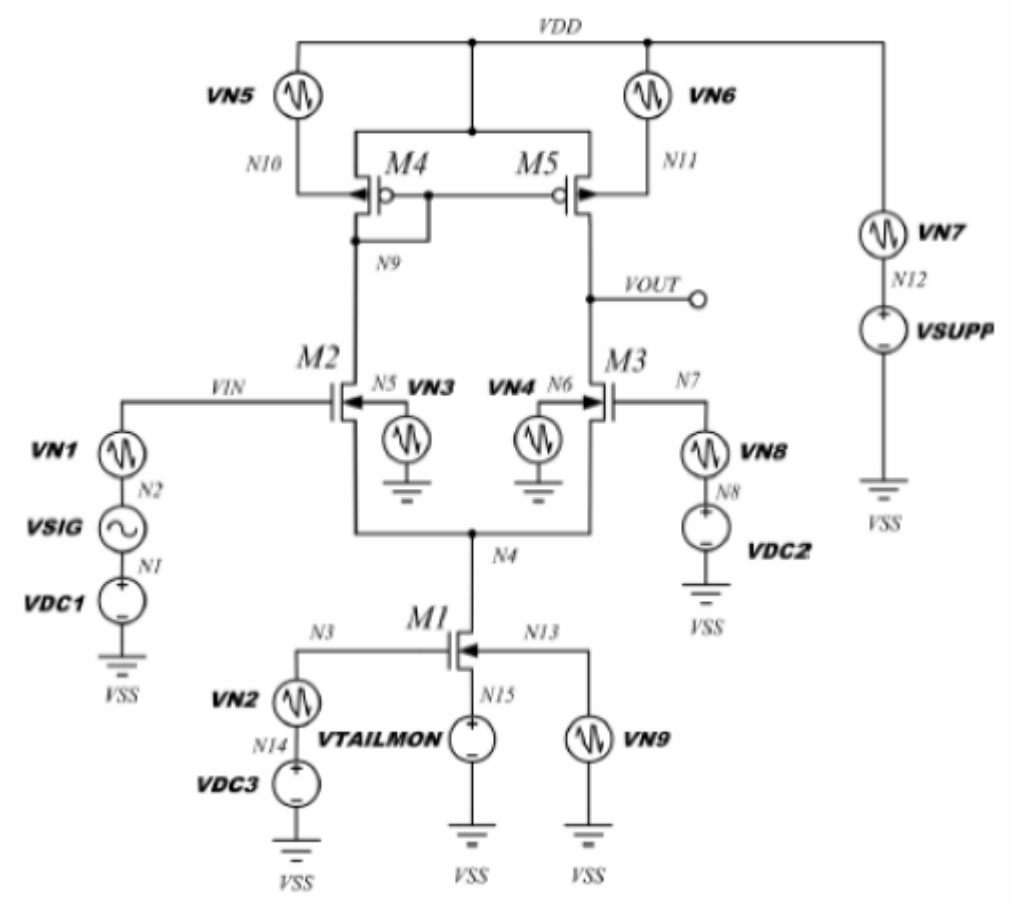


Fig. 5.1

b). Increase the low-frequency voltage gain of the circuit by rescaling the gate lengths of the transistors. Adjust the gate lengths by varying the parameters LTAIL, LP, and LN. You should easily obtain Au>400. Plot the frequency response of your final design. Determine the low-frequency voltage gain, and the -3dB bandwidth of the circuit. Give your new values for LTAIL, LP, and LN.

[HINT: Use simulator command .step PARAM to vary the parameters. None of the gate lengths should be shorter than 1.0 um or longer than 8 um.]

c). Now, modify your rescaled circuit to the circuit of Figure 6.2. You do not need to remove supplies like VN1-VN9 from the netlist, just set them to zero volts. All you need to do is to disconnect the gate circuit of M3 and then add M6, M7, R1, R2, VDC4 and VDC5. Use the following parameters for the new circuit elements:

M6: W=20um L=1um and M7: W=4um L=4um

VDC4: DC 1.6V and VDC5: DC 1.2V

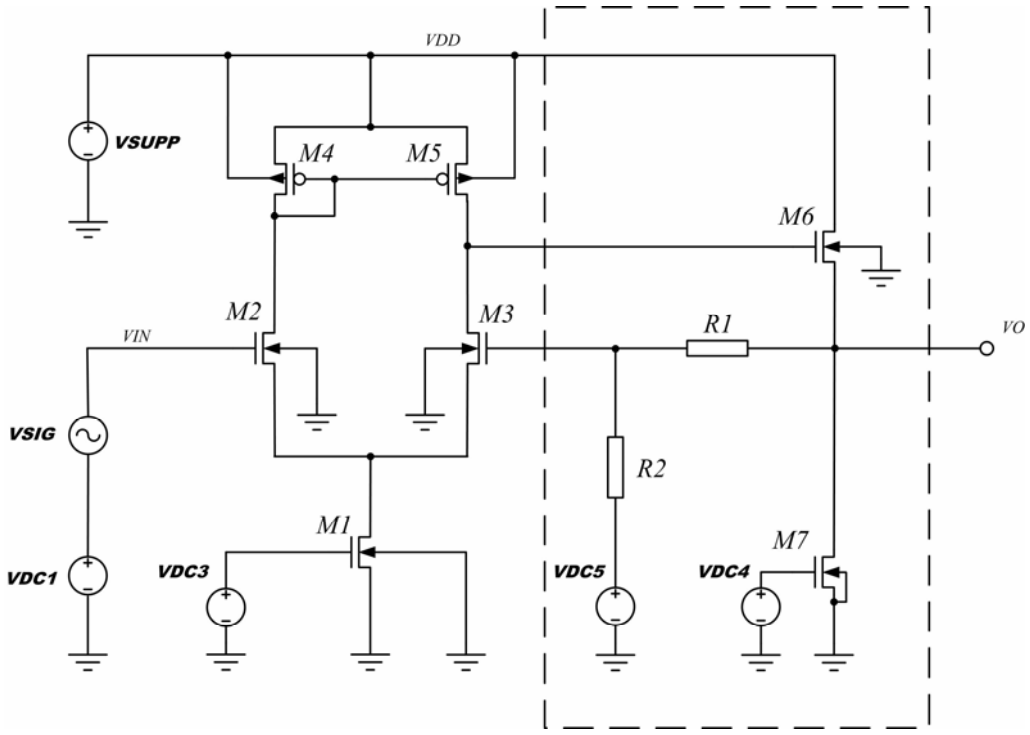


Fig. 5.2

In this circuit, M6 acts as a source follower with an active load M7. The resistor network feeds back a sample of the output voltage VO to the negative input of the differential gain block.

Set R1=100kohm and R2=1 ohm. Plot the frequency response of the circuit. Estimate the -3dB frequency.

d). Set R1=10kohm and R2=1 kohm. Simulate and plot the magnitude response of the circuit. Estimate the -3dB frequency.

e). Set R1=100kohm and R2=10 kohm. Simulate and plot the magnitude response of the circuit. Estimate the -3dB frequency.

f). (Voluntary) Calculate the product of the -3dB frequency and Au in c), d) and e). Can you explain the differences?

SPICE code:

```
* noisyamp.cir v. 1.0 020205JT
*
* A simple CMOS voltage gain stage. NOTE This is not a good
* amplifier design, but was designed to show how to simulate
* transfer functions, time domain response, and noise coupling
*
* VSUPP = the supply voltage source
* VSIG = the signal source
* VN1-VN9 = potential noise sources
* VDC1-VDC3 = bias voltage sources
* VTAILMON 0V source for monitoring the tail current of the differentilal stage.

.INCLUDE CMOS_SUBMIC.MOD
.CONNECT VSS 0
.PARAM VDCIN=1.2
.PARAM VDCTAIL=1.6
.PARAM WN=10u
.PARAM LN=0.5u
.PARAM WTAIL=4u
.PARAM LTAIL=0.6u
.PARAM WP=20u
.PARAM LP=0.5u
VSUPP N12 VSS DC 3
VSIG N2 N1 DC 0 SIN(0 1m 1k 0 0)
VTAILMON N15 VSS DC 0

* The bias sources
VDC1 N1 VSS DC VDCIN
VDC2 N8 VSS DC VDCIN
VDC3 N14 VSS DC VDCTAIL

* The noise soures
VN1 VIN N2 DC 0 AC 1
VN2 N3 N14 DC 0
VN3 N5 VSS DC 0
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VN4 N6 VSS DC 0
VN5 N10 VDD DC 0
VN6 N11 VDD DC 0
VN7 N12 VDD DC 0
VN8 N7 N8 DC 0
VN9 N13 VSS DC 0

* The transistor circuit
M1 N4 N3 N15 N13 MN L=LTAIL W=WTAIL
M2 N9 VIN N4 N5 MN L=LN W=WN
M3 VOUT N7 N4 N6 MN L=LN W=WN
M4 N9 N9 VDD N10 MP L=LP W=WP
M5 VOUT N9 VDD N11 MP L=LP W=WP

* The output load capacitance
*Cload VOUT VSS 1p
* Analysis
*.op
*.tran 1u 10m 0 1u
*.plot v(VIN) v(VOUT)
* step the input DC component to see the effect of signal dependent operating points
.step param VDCIN 1.1 1.3 0.05
.ac dec 50 1 1G
.plot ac vm(VOUT)
.end
```