TFE 4200 Analog Integrated Circuits
Problem sheet #3

1. At 0.1 Hz, a low-frequency measurement has a noise value of -60dBm when a resolution bandwidth of 1mHz is used. Assuming 1/f noise dominates, what would be the expected noise value in dBm over the band from 1 mHz to 1 Hz?

2. Consider an inductor of value L and an arbitrary resistor in parallel, as shown in Fig.1. Show that the current noise, $i_{no}(t)$, has a noise value given by

$I^2_{no}(rms) = KT/L$

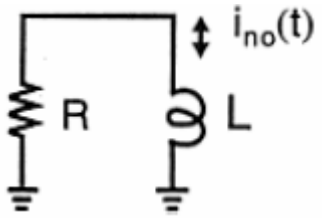

Fig. 1

3. Find the maximum thermal output noise voltage that the gate resistance(R_G) of a single MOSFET can generate.
[Hint: Assume a total distributed gate resistance is R_G, transconductance of MOSFET is gm and output resistance is r_{ds}]

4. Find the maximum output noise voltage that a single MOSFET, which has a transconductance of gm and output resistance is of r_{ds} and aspect ratio of W/L can generate.
[Hint: Include flicker noise and thermal noise. Maximum output noise occurs if the transistor sees it's own output impedance as the load]

5. For a 100μm/0.5μm MOS device with gm = 1/(100 Ω), the 1/f noise corner frequency is measured to be 500kHz, If t_{ox} = 90A^0, what is the flicker noise coefficient, K, in this technology?

6. Calculate the input-referred thermal noise voltage of the amplifier shown in Fig.2, assuming both transistors are in active region. Also, determine the total output thermal noise if the circuit drives a load capacitance C_L. What is the output signal-to-noise ratio if a low-frequency sinusoid of amplitude V_M is applied to the input.

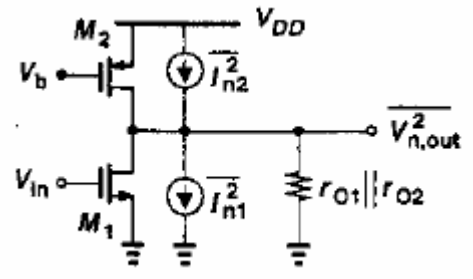

Fig. 2

7. The circuit shown in Fig.3 is designed for amplifying a weak single-ended voltage signal from an acoustic sensor. Spice code including the transistor model is also given below.

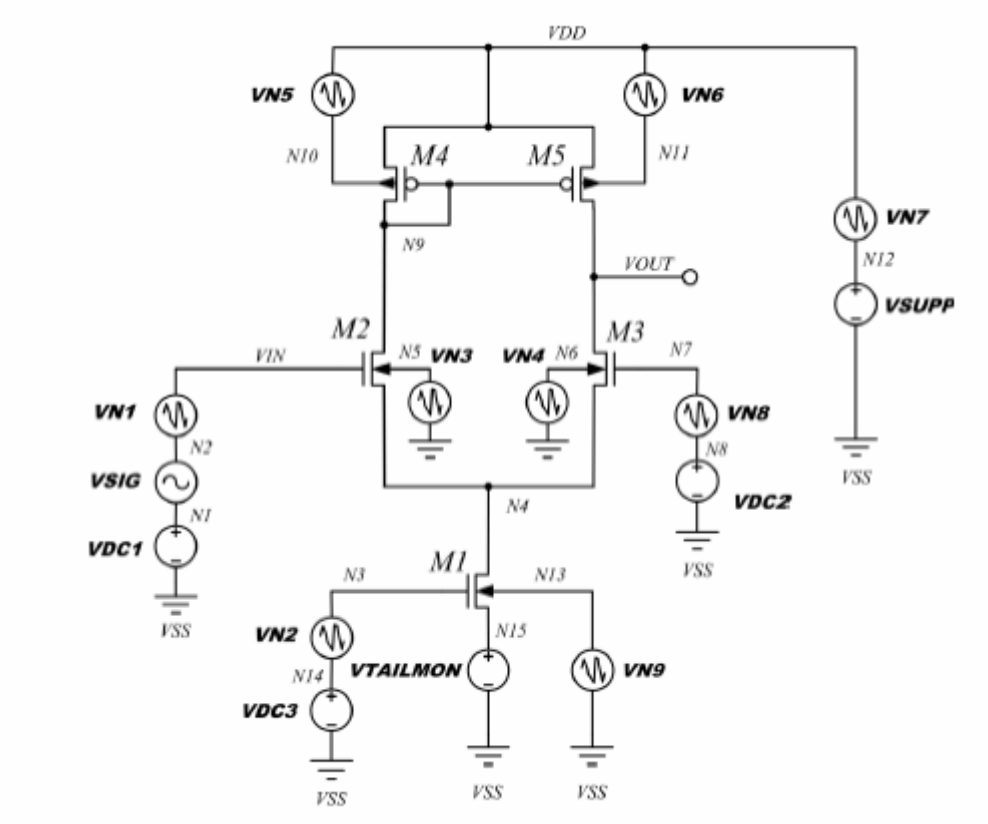

Fig. 3

1) Voltage sources VN1-VN9 represent the potential noise coupling points in the circuit. Plot the ac response from each noise source to the output VOUT (one plot for each noise source).

2) The amplifier is driven from the signal source VSIG with a 1 mV rms signal. Assume that in the supply voltage there is a 7 mVrms white noise signal and that there is another uncorrelated 0.2 mV rms white noise source in the bias source VDC2. You can ingnore all other noise sources. Calculate the signal-to-noise ratio in the output of the amplifier.

3) Simulate the ac response from noise sources in the gates of M4 and M5 to the output.

NOTE: For this simulation, you must modify the circuit netlist by adding new voltage sources in series with the gates of M4 and M5. Compare the sensitivity of M4 and M5 gates to the gates of M2 and M3. Is the difference significant?

SPICE code:

```
* noisyamp.cir v. 1.0 020205JT
*
* A simple CMOS voltage gain stage. NOTE This is not a good
* amplifier design, but was designed to show how to simulate
* transfer functions, time domain response, and noise coupling
*
* VSUPP   = the supply voltage source
* VSIG    = the signal source
* VN1-VN9 = potential noise sources
* VDC1-VDC3 = bias voltage sources
* VTAILMON 0V source for monitoring the tail current of the differentilal stage.

.INCLUDE CMOS_SUBMIC.MOD
.CONNECT VSS 0

.PARAM VDCIN=1.2
.PARAM VDCTAIL=1.6
.PARAM WN=10u
.PARAM LN=0.5u
.PARAM WTAIL=4u
.PARAM LTAIL=0.6u
.PARAM WP=20u
.PARAM LP=0.5u

VSUPP N12 VSS DC 3
VSIG N2 N1 DC 0 SIN(0 1m 1k 0 0)
VTAILMON N15 VSS DC 0

* The bias sources
VDC1 N1   VSS DC VDCIN
VDC2 N8   VSS DC VDCIN
VDC3 N14 VSS DC VDCTAIL

* The noise soures
VN1 VIN N2  DC 0  AC 1
VN2 N3  N14 DC 0
VN3 N5  VSS DC 0
VN4 N6  VSS DC 0
VN5 N10 VDD DC 0
VN6 N11 VDD DC 0
VN7 N12 VDD DC 0
VN8 N7  N8  DC 0
VN9 N13 VSS DC 0

* The transistor circuit
M1 N4   N3  N15 N13 MN L=LTAIL W=WTAIL
M2 N9   VIN N4  N5  MN L=LN    W=WN
M3 VOUT N7  N4  N6  MN L=LN    W=WN
M4 N9   N9  VDD N10 MP L=LP    W=WP
```

```
M5 VOUT N9  VDD N11 MP L=LP    W=WP

* The output load capacitance
*Cload VOUT VSS 1p

* Analysis
*.op
*.tran 1u 10m 0 1u
*.plot v(VIN) v(VOUT)

* step the input DC component to see the effect of signal dependent operating points
.step param VDCIN 1.1 1.3 0.05

.ac dec 50 1 1G
.plot ac vm(VOUT)

.end
```