TFE 4200 Analog Integrated Circuits

Problem sheet #2

1 a). Draw the small signal, high frequency model of a MOS transistor (NMOS or PMOS) when biased in the active region. Modify this small signal high frequency model to get a small signal, low frequency model. Define small signal parameters g_m, g_s and g_{ds}.

1 b). Draw the small-signal, low frequency T model of a MOS transistor (NMOS or PMOS) when biased in the active region (Ignore the body effect).

2. Fig. 1 shows the demonstrations of saturation and triode regions for an NMOS transistor. Draw the same demonstrations for a PMOS transistor.

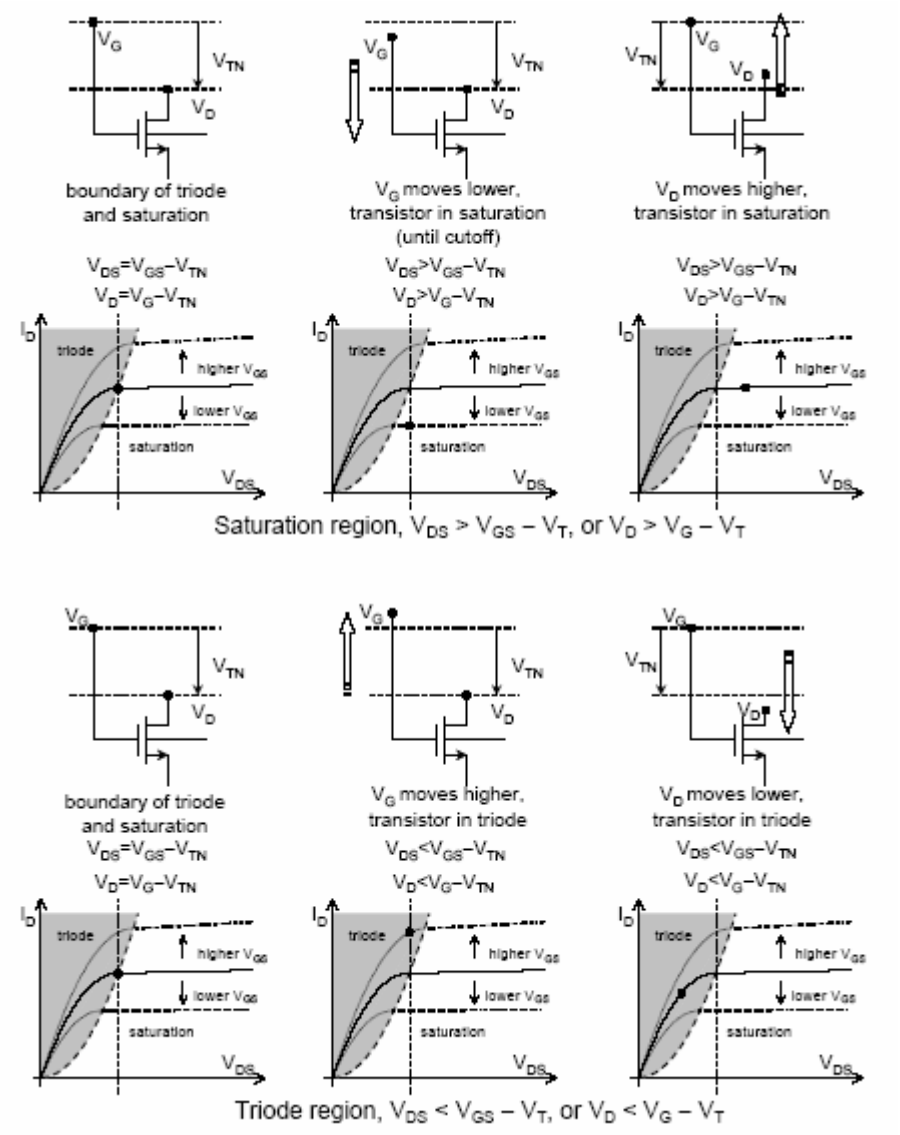

Fig. 1. Demonstrations of saturation and triode regions for an NMOS transistor

3. Find the capacitances C_{gs}, C_{gd}, C_{db} and C_{sb} for an active transistor having W=50 μm and L=1.2 μm. Assume that the source and drain junctions extend 4 μm beyond the gate, resulting in source and drain areas being As = Ad = 200 μm^2 and the perimeter of each being Ps = Pd = 58 μm.
Cj = **2.4×10^{-4} pF / μm^2**, **Cox = 1.9×10^{-3} pF / μm^2**, **Cj-sw = 2.0×10^{-4} pF / μm**
Cgs(overlap) = Cgd(overlap) = **2.0×10^{-4} pF / μm**

4. Consider the circuit shown in Fig. 2, where V_{in} is a dc signal of 1V. Taking into account only the channel charge storage, determine the final value of **V'** when the transistor is turned off, assuming half the channel charge goes to C_{hld}.

W/L of Q1 is **10 μm/ 0.8 μm**
C_{hld} = **1pF**
ϕ_{clk} = **5V**
C_{ox} = **1.9×10^{-3} pF / μm^2**
V_{tn} = **0.8 V**

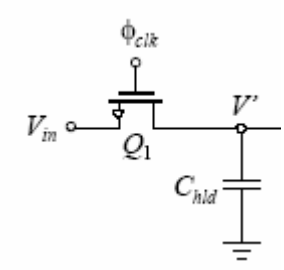

Fig. 2

5 a). For the circuit shown in Fig. 2, the input voltage has a step voltage change at time 0 from 1 V to 1.2 V (The gate voltage remains at 5 V). Find it's 99 percent settling time (the time it takes to settle to within 1 percent of the total voltage change).

Hint: Ignore the body effect ($V_{tn} = V_{t0}$) and ignore all capacitances except C_{hld}

W/L of Q1 is **10 μm/ 0.8 μm**
C_{hld} = **1pF**
ϕ_{clk} = **5V**
$\mu_n C_{ox}$ = **92 μA / V^2**
V_{tn} = **0.8 V**

b). Repeat for V_{in} changing from 3 V to 3.1 V.

6. Discuss the various non-ideal effects in a MOS transistor? How does the shape of VDS Vs. ID curves change? Explain the non-zero slope of VDS vs. ID curves. What implication does it have?

7. Plot the on-resistance of M1 as a function of V_G for the arrangement shown in Fig. 3.
W/L of M1 is **10**
$\mu_n C_{ox}$ = **50 μA / V^2**
V_{tn} = 0.8 V
[Hint: Drain terminal is open which indicates $I_D = 0$ so $V_{DS} = 0$]

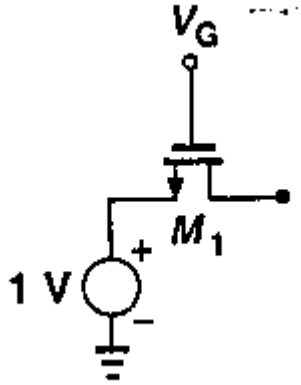

Fig. 3

8. Plot the g_m as a function of V_{DS} for the arrangement shown in Fig. 4.
[Hint: Express g_M in terms of V_{DS}]

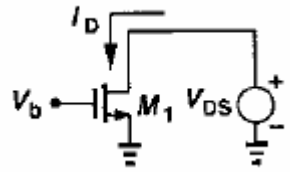

Fig. 4

9. Plot the drain current if V_X varies from -α to 0.
V_{tn0}=0.6 V, γ = 0.4 V$^{1/2}$ and $2\phi_F$ = 0.7 V
[Hint: Body effect]

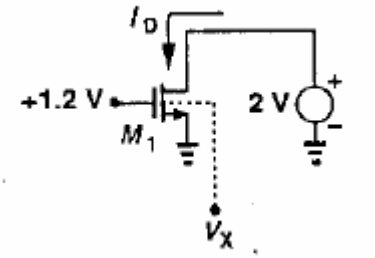

Fig. 5

10. Plot g_m and g_s as a function of I_1 for M1 shown in Fig. 6.
[Hint: Express g_m in terms of I_1]

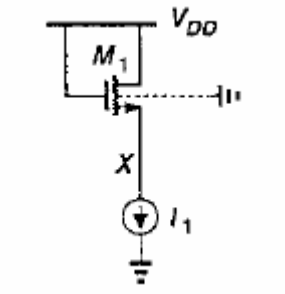

Fig. 6