TFE 4200 Analog Integrated Circuits

Problem sheet #1

1. A voltage amplifier has a frequency response of the low-pass STC(Single Time Constant) type with a dc gain of 60dB and a 3-dB frequency of 1 kHz. Find the gain in dB at f=10Hz, 100Hz, 1000Hz, 10kHz, 100kHz and 1MHz.

2. Fig. 1 shows the transconductance amplifier with Ri= 5KΩ, Ro=50KΩ and Gm=10 mA/V. If the amplifier load consists of a resistance R_L in parallel with C_L then show that the transfer function V_o/V_i, is of the low pass STC(Single Time Constant) type. Find the lowest value of R_L such that the dc gain is of at least 40dB. With this value of R_L connected, find the highest value of C_L so that the 3-dB bandwidth of at least 100kHz is obtained.

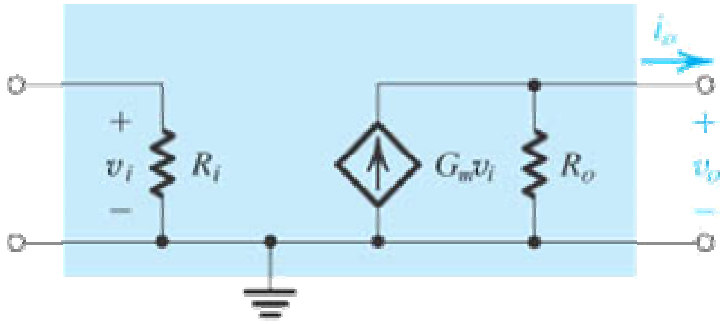

Fig. 1

3. Find the transfer function V_2/V_S for the circuit shown in Fig. 2 and show that it is of high pass STC(Single Time Constant) type. What is the smallest value of C that will ensure that the 3-dB frequency is not higher than 100 Hz.

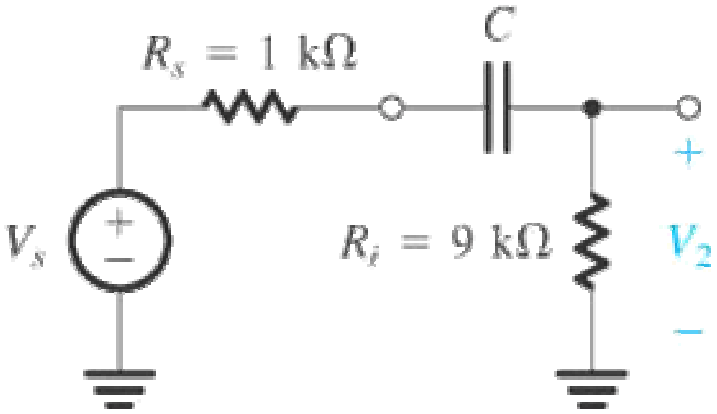

Fig. 2

4. The unity-gain voltage amplifiers in the circuit of Fig. 3 have infinite input resistances and zero output resistances and thus function as perfect buffers. Find the expression for the transfer function V_o/V_i. Find the 3-dB frequency in terms of RC.

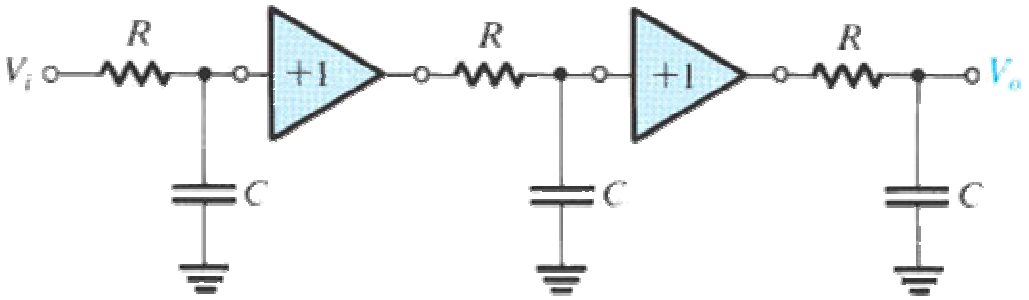

Fig. 3

5. An internal node of a high frequency amplifier whose Thevenin-equivalent node resistance is 100kΩ is accidentally shunted to ground by a capacitor (i.e., the node is connected to ground through a capacitor) through a manufacturing error. If the measured 3-dB bandwidth of the amplifier is reduced from 6 MHz to 120kHz, estimate the value of the shunting capacitor. If the original cutoff frequency can be attributed to a small parasitic capacitor at the same internal node (i.e., between the node and ground), what would you estimate the parasitic capacitance to be?

6. A designer wishing to lower the overall upper 3-dB frequency of a three-stage amplifier to 10kHz considers shunting one of the two nodes: Node A, between the output of the first stage and the input of the second stage and node B, between the output of the second stage and the input of the third stage, to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she shunts a capacitor of 1 nF, first to node A and then to node B, lowering the 3-dB frequency from 2MHz to 150KHz and 15KHz, respectively. If she knows that each amplifier stage has an input resistance of 100kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should be connected to which node to solve her design problem most economically?

7. SPICE simulation

Draw the equivalent schematic circuit for the following netlist and extract the DC gain by simulating using SPICE.

*** NETLIST ***

```
Vdd 1 0 dc 5
Ibias 2 0 dc 100u
M3 2 2 1 1 pmos w=100u l=1.6u
M2 3 2 1 1 pmos w=100u l=1.6u
M1 3 4 0 0 nmos w=100u l=1.6u
Vin 4 0 dc 0.890 ac 1

.MODEL nmos NMOS   LEVEL=3,      TOX=1.8E-8,     LD=0.08U,
+            UO=500,    VMAX=2.0E5,       PHI=0.6,

+             GAMMA=0.5,     NSUB=2.5E16,       VTO=0.7,
+            NFS=8.2E11,       CGSO=2.5E-10,     CGBO=2.5E-10,
+            CJSW=2.5E-10,  CGDO=2.5E-10,       MJ=0.5,
+            CJ=2.5E-4,    PB=0.9,     IS=1.0E-16,
+            JS=1.0E-4     KF=600E-27       AF=0.8
+                  RS=600       RD=600
+            ETA=0.05   KAPPA=0.007        THETA=0.06
+                  XJ=2.7E-7    DELTA=0.7

.MODEL pmos PMOS   LEVEL=3,      TOX=1.8E-8,     LD=0.08U,
+            UO=165,    VMAX=2.7E5,       PHI=0.80,

+             GAMMA=0.75,    NSUB=5.5E16,       VTO=-0.7,
+            NFS=7.6E11,       CGSO=2.5E-10,     CGBO=2.75E-10,
+            CJSW=3.4E-10,  CGDO=2.5E-10,       MJ=0.5,
+            CJ=3.7E-4,        PB=0.8,       IS=1.0E-16,
+             JS=1.0E-4     KF=400E-27     AF=1.0
+                  RS=1200      RD=1200
+            ETA=0.12    KAPPA=1.5    THETA=0.135
+                  XJ=2.3E-7    DELTA=0.3
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Hint: Adjust the DC gate voltage of transistor, M1, such that DC output voltage (i.e. voltage at node 3) will be roughly in the middle (around 2.5) of supply voltage (5V) and then plot the frequency response.