TFE4186 Analog CMOS 1
Øving 2

Problem 1 (8.2):

For the T/H if Fig.1, assume V_{in} is a 20MHz sinusoid with $2V_{p-p}$ amplitude. Also assume that ϕ_{clk} is a 100MHz square wave having a peak amplitude of $\pm 2.5V$ with rise and fall times 0f 1.5ns. What is the maximum time difference between the turn-off times of the n-channel and p-channel transistors? Ignore the body effect.

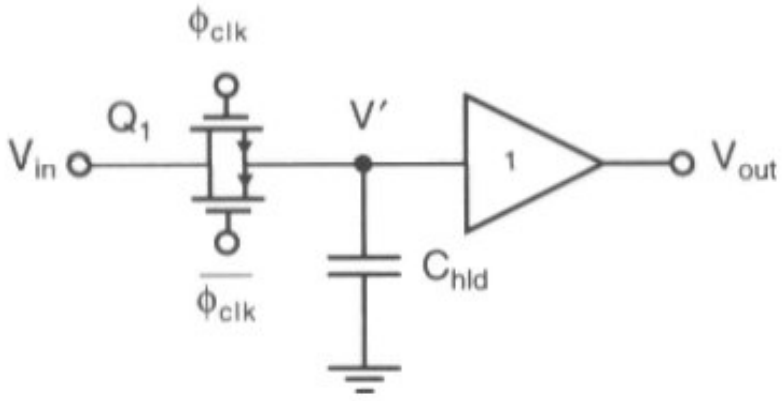

Fig. 1 (Problem 1)

Problem 2 (8.3):

The T/H of Fig.2 has transistors that are $10\mu m/0.8\mu m$ and 1pF hold capacitor. Assume the clock waveforms are fast enough that the channel charge of the transistors is evenly distributed between the two junctions. Compare the final hold pedestal between the case when the dummy switch turns on substantially before the sampling switch turns off, and the case when it turns on substantially after the sampling switch.

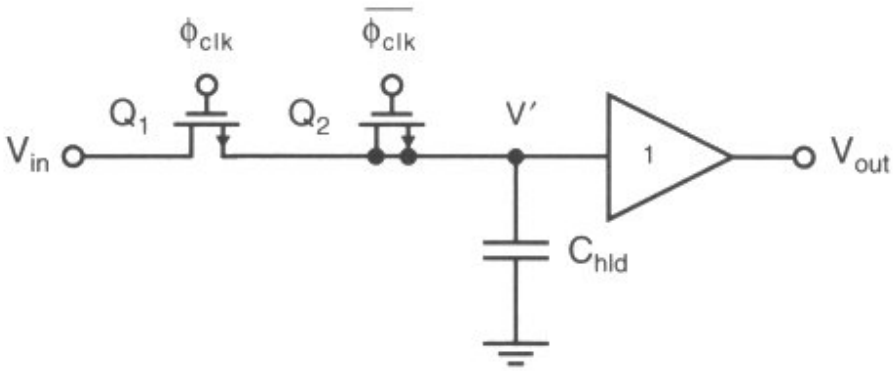

Fig. 2 (Problem 2)

Problem 3 (8.7):

Derive the output voltage of the S/H of Fig. 3 at the end of ϕ_2 in terms of the input voltage at the end of ϕ_1, the output voltage at the end of ϕ_1 from the previous period, and the capacitor ratio C_1/C_2. Take the z-transform of this difference equation, and substitute $z = e^{j\omega t}$ to find the frequency-domain transfer function of the S/H. Making the assumption that $e^{j\omega t} \equiv 1 + j\omega t$ for $\omega << (1/T) = f_{clk}$, where f_{clk} is the sampling frequency, show that:

$$f_{-3dB} \cong \frac{1}{2\pi}\frac{C_1}{C_2} f_{clk}$$

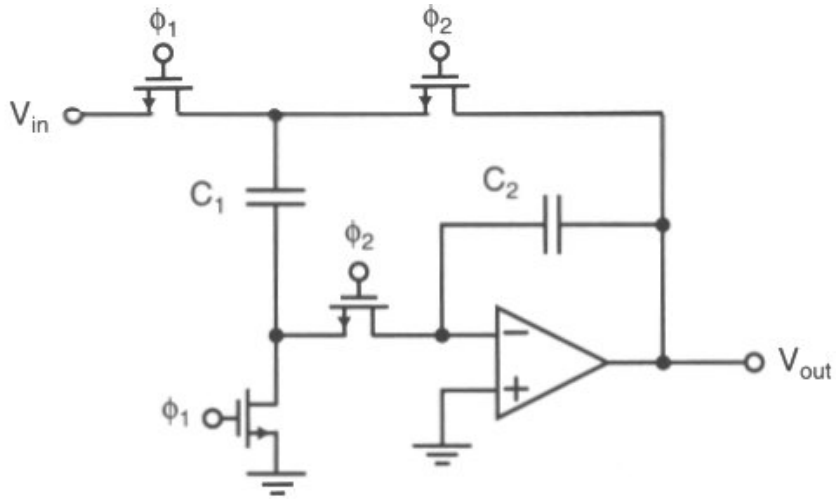

Fig. 3 (Problem 3)