Exercise 3

Problem 3.1:

Simulate the PMOS current mirror circuit of Figure 3.1 using AIM-spice. Use geometry parameters W=20 μm and L=2.0μm for both transistors, and the MOSFET model P1 that is described in the file '*modelcards_v30.cir'*.

a) Set the bias current I_{bias} = 50 μA, V_{DD}= 1.7 V, R_L=18 $k\Omega$. How much is the current I_{out}? How much is the output voltage V_{out}? ($I_{out} \approx 52\ \mu A$, $V_{out} \approx$ 0,9 V)
b) Use the same parameter values as in a), but set now V_{DD}= 2.3 V. How much are I_{out} and V_{out} now? ($I_{out} \approx 56\ \mu A$, $V_{out} \approx$ 1 V)
c) Use the same parameter values as in a), but set now R_L=12 $k\Omega$ and V_{DD}= 1.7 V. How much are I_{out} and V_{out} now? ($I_{out} \approx 54\ \mu A$, $V_{out} \approx$ 0.6 V)
d) Calculate the output impedance $r_{out} = |\Delta V_{out}/\Delta I_{out}|$ of the current mirror circuit based on the results from a) and c) ($r_{out} \approx 130$ kΩ). What is the Power Supply Rejection Ratio of this circuit (PSRR ≈ 0.1)? PSRR is defined as PSRR $=\Delta V_{out}/\Delta V_{DD}$.
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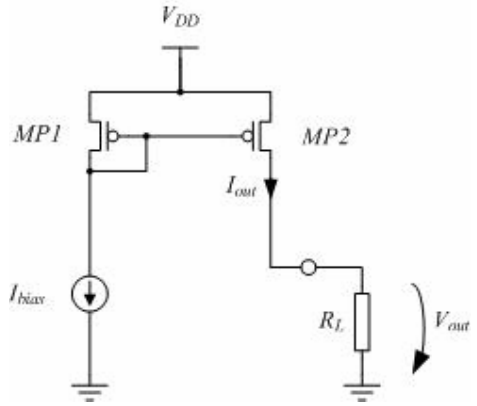

Figure 3.1

Problem 3.2:

Simulate the current mirror circuit of Figure 3.2 using AIM-spice. Use geometry parameters W=20 μm and L=2.0μm for all the four transistors, and the MOSFET model P1 that is described in the file '*modelcards_v30.cir'*.

a) Set the bias current I_{bias} = 50 μA, V_{DD}= 2.0 V, R_L=18 $k\Omega$. How much are I_{out} and V_{out} ? ($I_{out} \approx 50\ \mu A$, $V_{out} \approx$ 0.9 V)

b) Use the same parameter values as in a), but set now V_{DD}= 2.3 V. How much are I_{out} and V_{out} now? ($I_{out} \approx 50\ \mu A$, $V_{out} \approx$ 0.9 V)

c) Use the same parameter values as in a), but set now R_L=12 $k\Omega$ and V_{DD}= 2.0 V. How much are I_{out} and V_{out} now? ($I_{out} \approx 50\ \mu A$, $V_{out} \approx$ 0.6 V)

d) What is the output impedance r_{out} of this circuit? ($r_{out} \approx 6\ M\Omega$)
What is the PSRR of this circuit? (PSRR < 0.01)
Compare the results in this problem with the results of Problem 3.1.

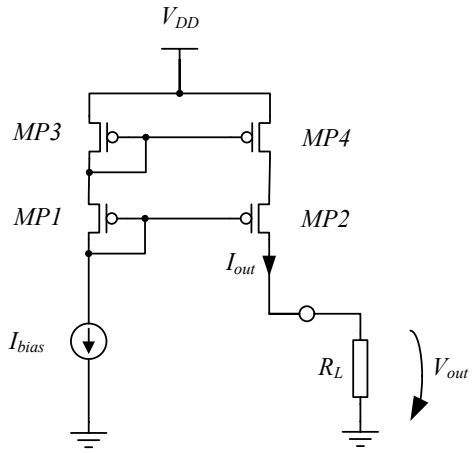

Figure 3.2

Problem 3.3:

The source follower circuit of Figure 3.3 has the following parameters:

W/L = 100 µm/1.6 µm
$\mu_n C_{ox}$ = 90 µA/V^2
$\mu_p C_{ox}$ = 30 µA/V^2
I_{bias} = 100 µA
γ_n = 0.5 V$^{1/2}$
$r_{ds\text{-}n}$ (Ω) = 8000L(µm)/I_D(mA)
V_{SB} = 2 V
R_{in} = 180 kΩ
C_L = 0.5 pF
C_{gs1} = 0.2 pF
C_{gd1} = 15 fF
C_{sb1} = 40 fF
C_{in} = 30 fF

a) Find the output impedance of the source follower at low frequencies.
b) Find the voltage gain of the circuit at low frequencies.

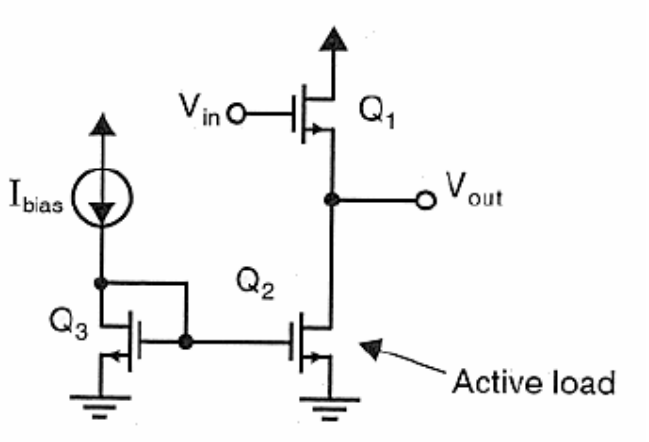

Figure 3.3